

Feasibility Demonstration of a High-Resolution
Integrated Optical
Analog-to-Digital Converter
(Patent Pending)

*R. J. Pieper, P. E. Pace, J. P. Powers
R. Van de Viere, C. C. Foster
R. Walley and H. Yamakoshi*

Department of Electrical and Computer Engineering
Naval Postgraduate School
Monterey, Ca. 93943
(408) 656-2101

Abstract

Recently, a new technique has been described for extending the resolution of an integrated optical multi-interferometer analog-to-digital converter (ADC) [1], [2]. These types of ADCs can directly digitize the signals from an antenna and play an important role in eliminating the need for intermediate frequency and baseband processing. With resolution greater than 12 bits, these types of architectures are useful for a variety of applications. The new technique is based on the incorporation of a symmetrical number system (SNS) encoding to provide high resolution (greater than 1-bit per interferometer) while also reducing the complexity of the optical hardware. In this paper we present our hardware design guidelines and apply these conditions to 14-bit and 8-bit architectures.

Introduction

With the increasing performance of modern shipboard equipment, the trend is to move the digital signal processing closer to the antenna and sensor systems. Digital microwave receivers and RF memories, for example, are expected to operate directly at X-band eliminating the need for intermediate-frequency and baseband processing. Integrated optical guided-wave ADC's play an important role in these types of systems since they can directly digitize the RF signals from the antenna.

The most efficient (sampling) ADCs demonstrated to date use integrated electro-optical guided-wave technology (in lithium niobate, gallium arsenide, or indium phosphide). Symmetrical folding of the input signal is realized with Mach-Zehnder Interferometric (MZI) waveguide modulators arranged in a parallel configuration [3, 4, 5, 6, 7]. These modulators use the linear Pockels effect and provide a convenient method for coupling a wideband electrical signal into an optical processing system through the modulator electrodes.

The technique for extending the resolution of an integrated optical multi-interferometer guided-wave ADC is shown in Figure 1. The input signal to each interferometer is symmetrically folded at twice a proper modulus. A small comparator ladder mid-level quantizes each interferometer's detected output to encode the analog signal in a symmetrical number system (SNS) for-

mat. By incorporating the SNS encoding, resolution greater than 1 bit per interferometer is provided. The dynamic range of a SNS system with N pairwise relatively prime moduli m_i is

$$D_r = \prod_i^N m_i. \quad (1)$$

Associated with each modulus is a uniquely configured folding circuit, employing a Mach-Zehnder interferometer, and a parallel bank of $(m_i - 1)$ comparators. The comparator outputs of thermometer code, represent the input signal in the SNS format. The final step in the process is assimilating the thermometer code to produce a digital output with a desired n bits of resolution. Perforce, the n bits of resolution should satisfy

$$2^n \leq D_r. \quad (2)$$

The folding circuit, which uses a Mach-Zehnder interferometer, is shown in Figure 2. The input RF, V_{in} , is stripped of DC to provide a bipolar implementation. The input RF signal is properly attenuated with a factor A_i in order to precondition the RF signal so that

$$V'_{in} = A_i(V_{in} - DC), \quad (3)$$

where a higher attenuation factor A_i corresponds to less applied attenuation ($A_i \leq 1$).

The laser diode produces an optical pulse train at greater the twice the Nyquist frequency. The input optical pulses sample the analog input signal so that

$$I = I_o \cos^2\left(\frac{\pi}{2} \frac{V'_{in}}{V_\pi} + \chi\right), \quad (4)$$

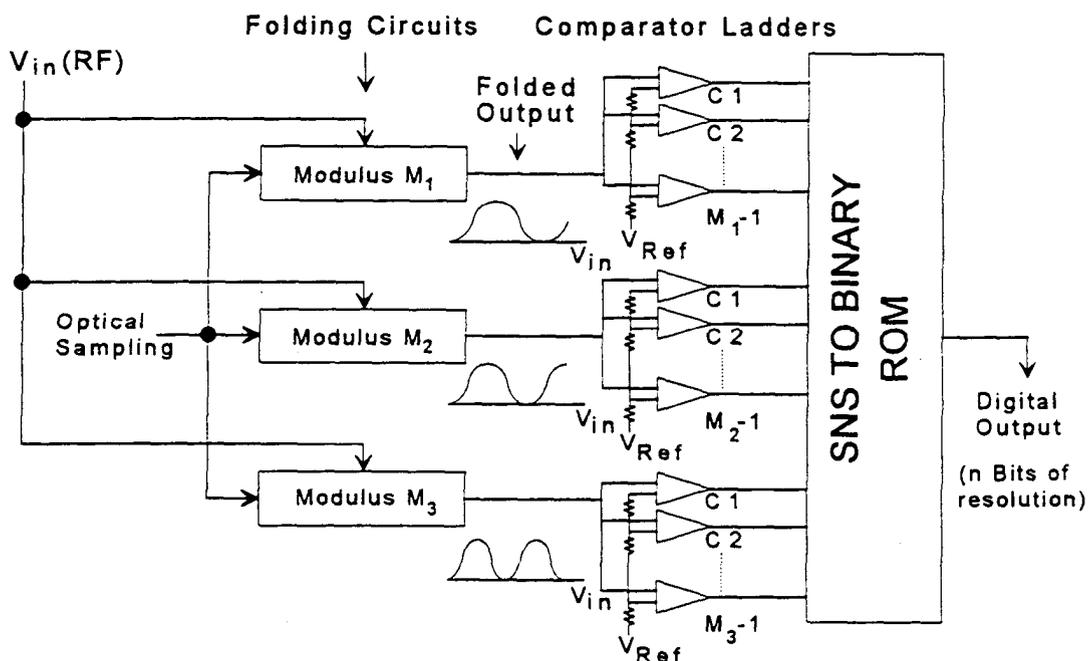


Figure 1. System overview of novel high resolution Analog-to-Digital converter

where I_0 is the maximum throughput optical intensity, V_π is a measure of the electrooptic sensitivity which depends on the optical wavelength and material constants, and χ is a fixed phase shift that adjusts the quadrature point to properly align the moduli. Another important parameter is the maximum input voltage, V_{\max} that can safely be applied to the MZI. The condition

$$|V'_{in}| < V_{\max} \quad (5)$$

puts a second upper limit on the system's n -bit resolution.

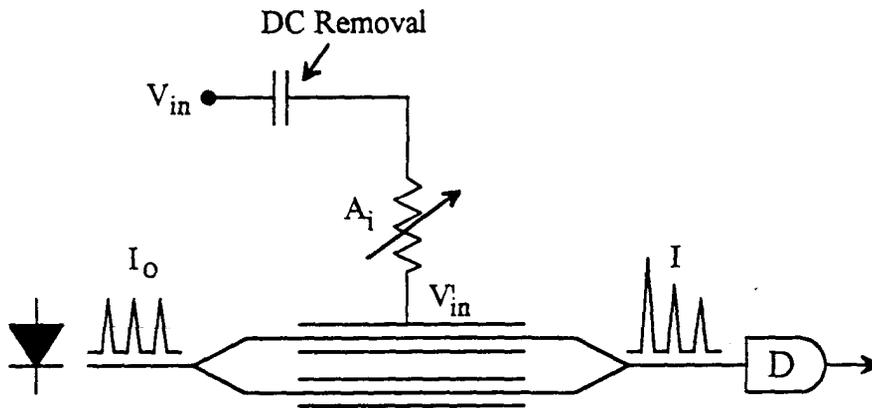


Figure 2. Typical folding circuit.

Figure 3 shows the definition for a modulus 3 folding waveform; also shown are the proper comparator threshold levels to mid-level quantize the input voltage. Figure 4 shows the comparator states for a $D_r = 12$ system that uses $m_1 = 3$ and $m_2 = 4$. The effect of the attenuation factor A_i in Figure 4 is to create an effective V_π of

$$V_\pi^{eff} = \frac{V_\pi}{A_i}. \quad (6)$$

The attenuation of the input signal allows the folding period to be scaled to the particular modulus.

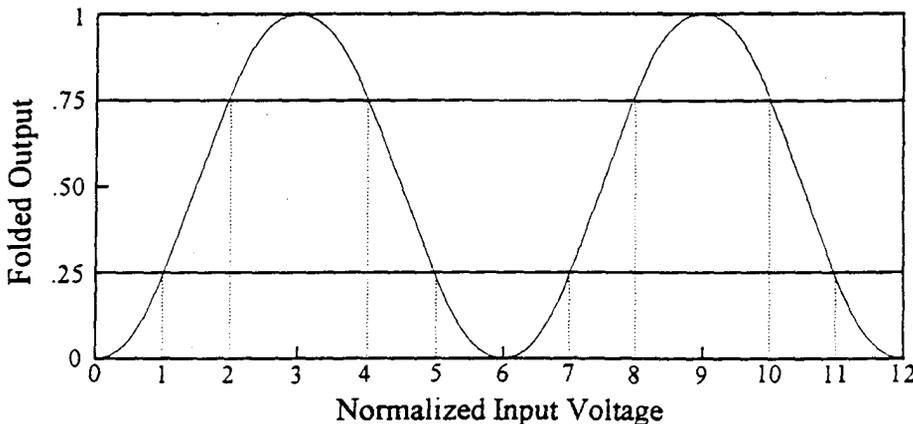


Figure 3. Modulus 3 Folding waveform.

The design rules for the SNS ADC are as follows. Considering a device with a specific V_π and V_{\max} , the maximum number of possible folds is computed as

Rule 1
$$(\# folds)_{\max} \leq \frac{V_{\max}}{V_\pi}.$$

The number of bits n and the minimum modulus m_i are then chosen to satisfy

Rule 2
$$D_r = (2^n - 1) < 2 m_i (\# folds)_{\max}.$$

From (1), the remaining $(n - 1)$ moduli are chosen to satisfy

Rule 3
$$D_r = \prod_{i=1}^N m_i.$$

Two examples are considered below.

Input	Folded Output SNS Moduli		Binary Code
	3	4	
0	0	0	0 0 0 0
1	1	1	0 0 0 1
2	2	2	0 0 1 0
3	2	3	0 0 1 1
4	1	3	0 1 0 0
5	0	2	0 1 0 1
6	0	1	0 1 1 0
7	1	0	0 1 1 1
8	2	0	1 0 0 0
9	2	1	1 0 0 1
10	1	2	1 0 1 0
11	0	3	1 0 1 1
12	0	3	1 0 1 1

Figure 4. A simple example with $D_r = 12$.

A 14 bit design

Consider an interferometer with $V_{\max} = 40$ volts and $V_\pi = 0.2$ volts. Rule (1) implies that $(\# folds)_i = 200$. Choosing $m = 14$, rule (2) implies that $m_1 = 41$. Using Rule (3), the moduli required are $m_1 = 41$, $m_2 = 42$ and $m_3 = 43$.

A 8 bit design

The specifications of the Mach-Zehnder interferometer available are: $V_{\max} \approx 30 \text{ v}$ and $V_{\pi} \approx 2 \text{ v}$. Rule (1) implies that $(\# \text{ folds}_i)_{\max} = 15$. Choosing $m = 8$, rule (2) implies that $m_1 = 9$. Using Rule (3) implies then that $m_1 = 9$, $m_2 = 10$ and $m_3 = 11$.

Hardware constructed for the 8-bit system

The 8-bit system requires folding circuits which correspond to moduli 9, 10 and 11. A comparator ladder for a moduli 10 is shown in Figure 5. Each priority encoder converts the $(m-1)$ on/off level comparator outputs to a compact 4-bit representation.

For the 8-bit design three priority encoders are needed (see Fig. 6). The binary word encoder integrates outputs from each priority encoder to produce a 10-bit binary word. The electronic hardware is configured to exercise 100% of the architecture's capabilities. Note that it would require 10 bits on the output to represent 990 states. The device limitations (V_{π} , V_{\max}) of the MZI reduce the practical application range to 80% of the dynamic range.

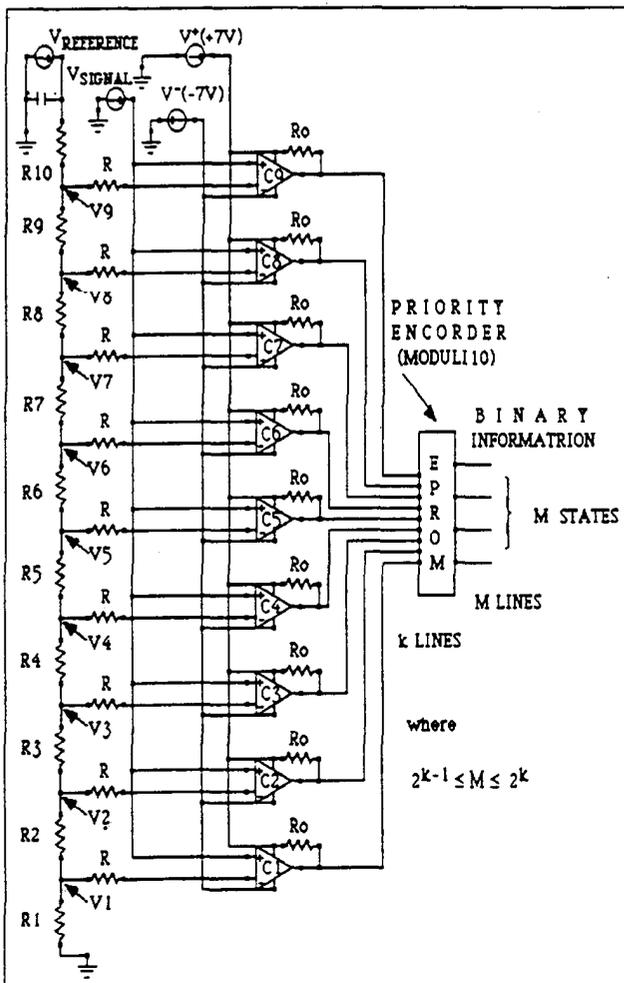


Figure 5. Comparator circuit for moduli 10

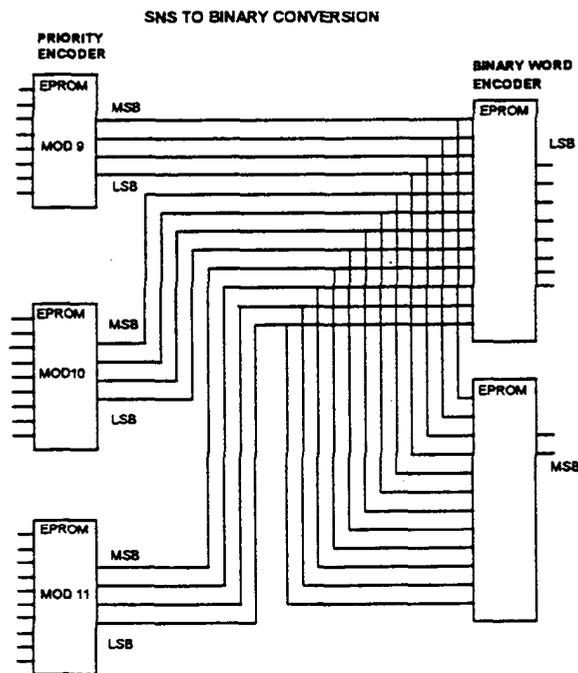


Figure 6. SNS to binary conversion

Conclusions

With regard to the 8-bit design, the MZI has been successfully tested with the moduli 10 priority encoder and the binary-word encoder. In addition the digital hardware for the SNS to binary conversion has been built and tested. The originally proposed 14-bit design will depend on a MZI with at least a 200 fold capability.

Acknowledgments

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