

Optical  $\Sigma\Delta$  Analog-to-Digital Converters for  
High-Resolution Digitization of Antenna Signals

*P.E. Pace, S.J. Ying, J.P. Powers, R.J. Pieper*

Department of Electrical and Computer Engineering  
Naval Postgraduate School Monterey, CA 93943  
E-mail: pace@pcpep.ece.nps.navy.mil  
Office: (408) 656-3286

Abstract

One of the major advantages of integrated optics is the capability to efficiently couple wideband antenna signals into the optical domain. High resolution integrated optical analog-to-digital converters (ADCs) based on symmetrical residues have been recently investigated to directly digitize the signal at the antenna [1,2]. This approach can provide on the order of 14-16 bits at fairly high sample rates.

Modern avionics equipment, such as super resolution direction-finding systems, now require resolutions on the order of 20 to 22 bits. Symmetrical residue converters are not feasible for this type of resolution. Using oversampling techniques based on sigma-delta ( $\Sigma\Delta$ ) modulation, a convenient tradeoff exists between sampling rate and resolution. That is, high resolution can be achieved with sampling rates much higher than the Nyquist rate. Typically,  $\Sigma\Delta$  processors require simple and relatively low-precision analog components and are well suited to integrated optical implementations.

In this paper we discuss the current  $\Sigma\Delta$  methodology, the advantages of optical integrated circuits and present a second-order integrated optical  $\Sigma\Delta$  architecture for direct antenna signal acquisition. Simulation design parameters and results are presented. Performance issues and future efforts are also considered.

Introduction

Oversampled ADC architectures offer a means of exchanging resolution in time for that in amplitude and represent an attractive approach to implementing precision converters without the need for complex precision analog circuits [3]. Converters based on  $\Sigma\Delta$  modulation employ integration and feedback in iterative loops to obtain high-resolution A/D conversions.

Block diagrams for first- and second-order  $\Sigma\Delta$  ADCs are shown in Fig. 1. The analog signal is sampled at well above the Nyquist frequency (oversampling) and fed through a quantizer via an integrator. The quantized output is then fed back and subtracted from the input. This feedback forces the average value of the quantized output to track the average value of the input signal. Any difference accumulates in the integrator and eventually corrects itself. When repeated at high speed, the quantizations are forced to oscillate between the quantized levels, keeping their running average representative of the input [4,5].

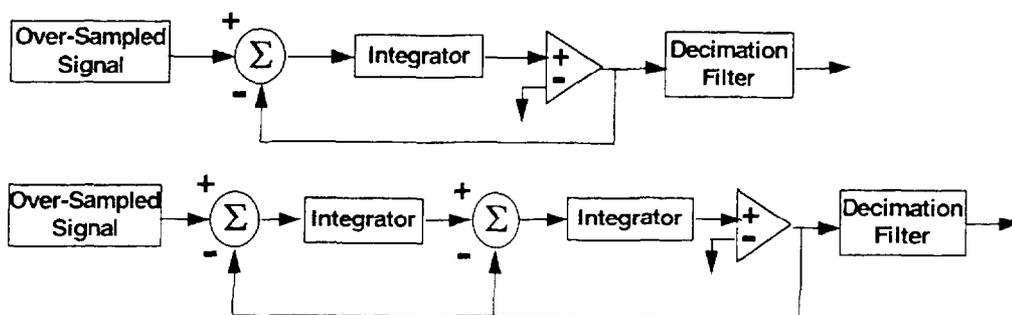


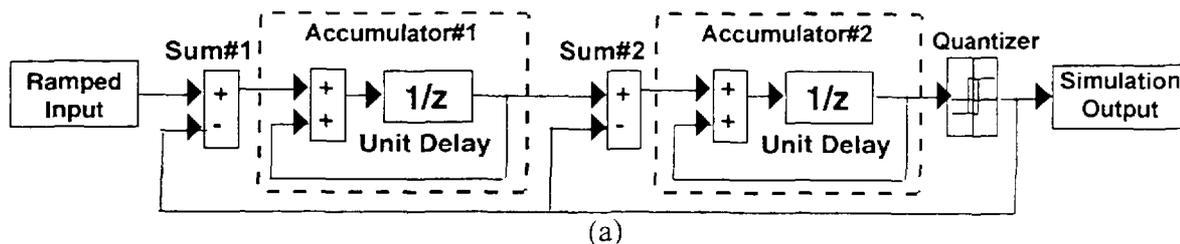
Fig. 1. First- and Second-Order  $\Sigma\Delta$  ADCs

Although the first-order model is the simplest, the quantization noise is highly correlated to the input [4]. Thus far, the second-order (two feedback loops)  $\Sigma\Delta$  modulator has proven to be the most stable and reliable. Higher-order designs suffer from instability due to the accumulation of large signals in the integrators [6]. The decimation filter (output block) is a low pass filter (LPF) which re-samples the quantized signal at the Nyquist rate. This serves to eliminate any out-of-band quantization noise. It also determines the ratio of the sampled, quantized outputs over the Nyquist interval. This average value proves to be highly representative of the input value.

### Second-Order $\Sigma\Delta$ Design and Simulation Results

To demonstrate the  $\Sigma\Delta$  concept, an all-electronic second-order converter was simulated as shown in Fig. 2a. The ramped input is modeled by a vector of sampled data values over a specific range. Each ideal discrete-time integrator is modeled as an accumulator in a unit-delay feedforward loop (using a z-domain transfer function).

From the plots (Fig. 2b) one can see that the duty cycles of the quantizer output are weighted toward the average value of the input. For example, at the start of the ramped input the duty cycles are weighted toward the bottom-level quantization. Towards the middle, the duty cycles are about 50%. At the high end of the ramp, they are weighted toward the top-level quantization. Figure 2b shows the signal value at the input and output of the accumulators. From the output of accumulator #1, it can be easily seen that the output is oscillating about the ramped input range of -2 to +2.



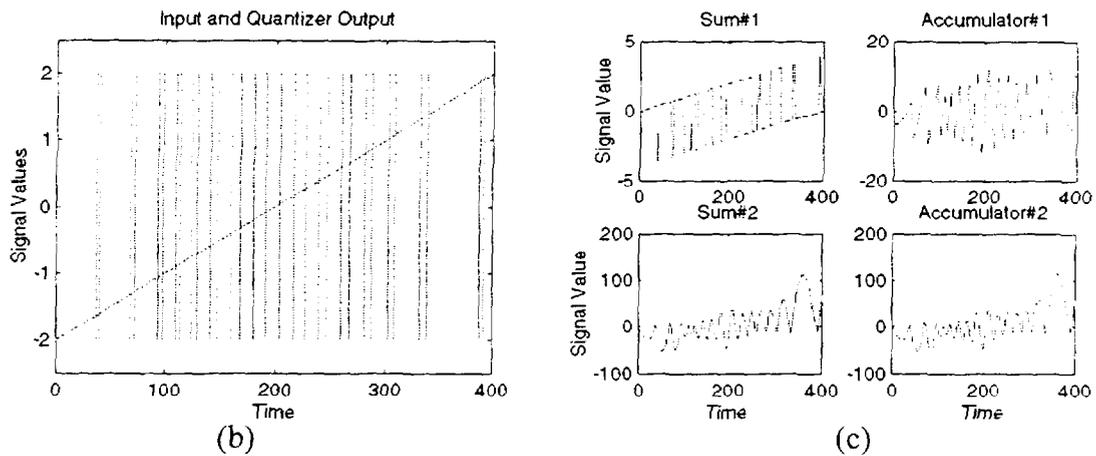


Fig. 2. (a) Electronic 2nd-Order  $\Sigma\Delta$  Converter Simulation Block Diagram. (b) Ramped Input and Quantizer Output. (c) First and second stages of converter.

### Electro-Optical Second-Order $\Sigma\Delta$ Architecture

Optical integrated circuits offer several advantages over conventional electronics. The large bandwidth offered by optical integrated circuits provides an attractive feature for oversampling techniques using conventional electronics, which usually are bandlimited to relatively low-frequency signals. Figure 3 shows a block diagram of a proposed electro-optical second-order  $\Sigma\Delta$  converter.

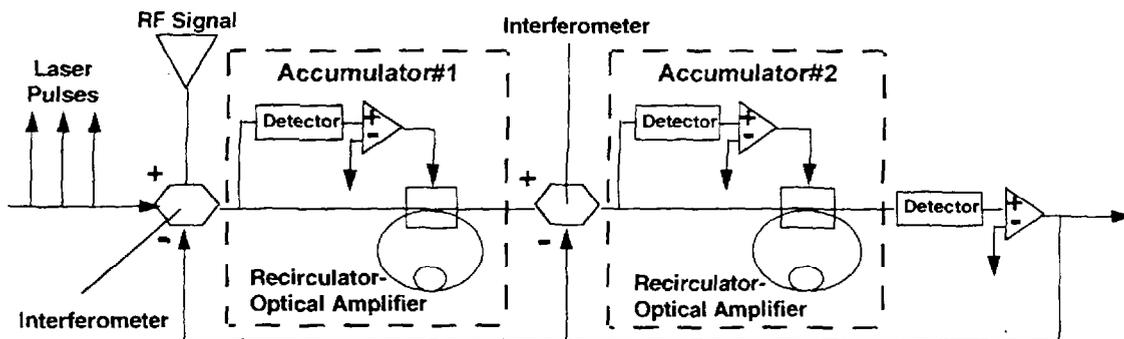


Fig. 3. Block Diagram of Integrated Optical Second-Order  $\Sigma\Delta$  Converter

In the electro-optic design, laser pulses from a mode-locked laser oversample the RF signal at the interferometer. Mode-locked lasers are capable of providing a high pulse repetition frequency, narrow pulse widths and jitter times on the order of 200 fs. The interferometer efficiently couples the wideband antenna signal into the optical domain. It also serves to subtract the feedback from the input signal. Figure 4 plots the normalized transfer characteristic of the interferometer. The operating region (input signal range) is chosen to be between -1 volt to 1 volt.

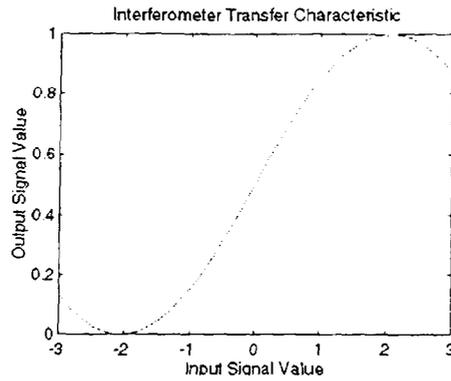


Fig. 4. Interferometer Transfer Characteristic

Since light intensity cannot be negative, the detectors and threshold comparators in Fig. 3 serve to control the direction of accumulation depending upon the signal strength. The recirculator accumulates downward if the output of the interferometer is less than 0.5 and upward for values greater than 0.5. Thus the detector, comparator and optical recirculator serve to function as an integrator.

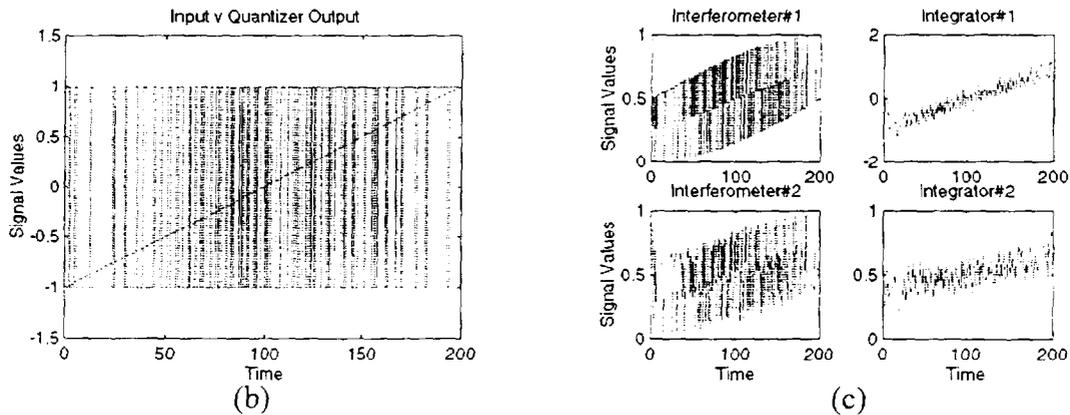
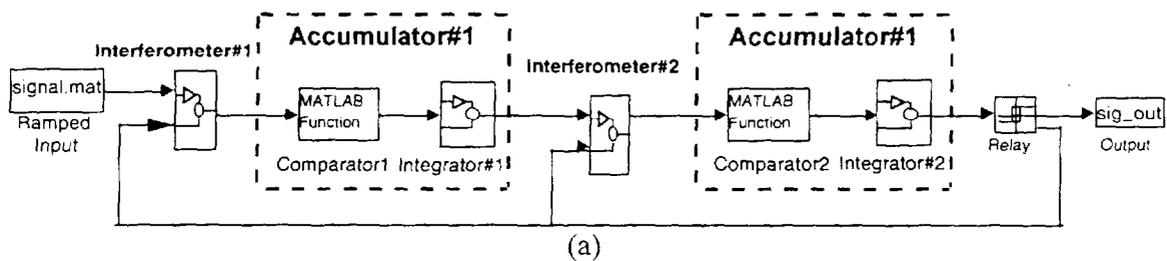


Fig. 5. Second-Order Integrated Optical  $\Sigma\Delta$  Converter  
 (a) SIMULINK Block Diagram  
 (b) Plot of Ramped Input and Quantized Output  
 (c) Plot of Accumulator Stages

The electro-optic  $\Sigma\Delta$  converter was simulated using MATLAB's SIMULINK toolbox (Fig. 5a). The average value of the quantizer output (Fig. 5b) can be seen to track the average value of the ramped input. The output of the interferometer (Fig. 5c) can be seen to oscillate about the ramped input. This comparison to the electronic design is only qualitatively since the decimation filter has yet to be included in the simulations.

### Conclusions

The  $\Sigma\Delta$  oversampling A/D converter architecture uses limit cycles in quantized feedback loops to provide an accurate digital representation of the input signal. The second-order  $\Sigma\Delta$  converter provides a stable and robust design that is highly tolerant of circuit imperfections and component mismatch. The main limitations of this method are fast cycle times and bandwidth.

An integrated optical second-order  $\Sigma\Delta$  architecture allows the processing of wideband RF signals. The electro-optic design is a fairly straight-forward modeling of the electronic design using standard integrated optical devices. Current simulation results confirm design feasibility.

Future efforts include further simulation of the optical implementation. Current design does not include a model for the recirculating optical delay lines nor reflect the performance of the optical amplifiers. Design issues to be studied include nonlinearities associated with interferometers, effects of net gains in the feedback loops, and the effects of modulation noise and oversampling frequency (OSR) on bit resolution.

### References

- [1] P.E. Pace and D. Styer, "High resolution encoding process for an integrated optical analog-to-digital convert," *Optical Engineering*, vol. 33, no. 8, pp. 2638-2645, 1994.
- [2] R.J. Pieper, P.E. Pace, J.P. Powers, R. Van de Veire and C.C. Foster, "Feasibility demonstration of a high-resolution integrated optical analog-to-digital converter," Proceedings of the PSAA-IV Fourth Annual ARPA Symposium on Photonic Systems For Antenna Applications, pp. 323-328, Jan. 1994.
- [3] J.C. Candy and G.C. Temes, "Oversampling methods for A/D and D/A conversion," J.C. Candy and G.C. Temes, editors, *Oversampling Delta-Sigma Data Converters*, IEEE Press, pp. 1-29, 1992.
- [4] B.E. Boser and B.A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.
- [5] J.C. Candy, "A use of limit cycle oscillations to obtain robust analog-to-digital converters," *IEEE Trans. Commun.*, vol. COM-22, pp. 298-305, March 1974.
- [6] J.C. Candy, "A use of double integration in sigma delta modulation," *IEEE Trans. Commun.*, vol. COM-33, pp. 249-258, Mar. 1985.